Claims

[c1] 1. An electronic chip, comprising:
a first circuit design module having a first grid; and
a second circuit design module having a second grid, wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in said fabrication.

[c2] 2. The electronic chip of claim 1, wherein at least one of said first grid and said second grid comprises a metallization grid.

[c3] 3. The electronic chip of claim 1, wherein said first grid and said second grid comprise one of a power grid and a ground grid.

[c4] 4. The electronic chip of claim 1, wherein said first grid and said second grid are interconnected by at least one of:
a diffusion region;
a gate of a field effect transistor;
a source of a field effect transistor connected to said first grid and a drain of said field effect transistor con-

nected to said second grid;
a local interconnect; and
a first metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

[c5] 5. The electronic chip of claim 1, wherein an interconnect between first grid and said second grid is conductive during said plasma processing and is non-conductive during an operation of said chip unless activated by a signal.

[c6] 6. The electronic chip of claim 1, wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip.

[c7] 7. The electronic chip of claim 6, wherein said chip includes a silicon on insulator (SOI) structure.

[c8] 8. The electronic chip of claim of claim 6, wherein said layer is temporarily activated by said plasma processing such that carriers in said layer are migratable during said plasma processing.

[c9] 9. The electronic chip of claim 2, wherein at least one of said first grid and said second grid comprises a metal grid that includes a predetermined surface area of at

least one of said first circuit design module and said second circuit design module.

[c10] 10. An electronic apparatus comprising:
an electronic chip fabricated in accordance with claim 1.

[c11] 11. A method of at least one of designing an electronic chip and fabricating said electronic chip, said method comprising:
interconnecting at least one grid of a design module of an electronic circuit formed on said chip with a corresponding grid in a second design module in a stage of fabrication of said chip such that a plasma processing of said fabrication does not cause a differential charge that damages a component of said chip.

[c12] 12. The method of claim 11, wherein at least one of first grid and said second grid each comprise a grid formed by metalization.

[c13] 13. The method of claim 11, wherein said first grid and said second grid comprise one of a power grid and a ground grid.

[c14] 14. The method of claim 11, wherein said first grid and said second grid are interconnected by at least one of:
a diffusion region;
a gate of a field effect transistor;

a source of a field effect transistor connected to said first grid and a drain of said field effect transistor connected to said second grid;
a local interconnect; and
a first metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

[c15] 15. The method of claim 11, wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip.

[c16] 16. The method of claim 15, wherein said chip comprises a silicon on insulator (SOI) structure.

[c17] 17. The method of claim of claim 11, wherein said layer is temporarily activated by said plasma processing such that carriers in said layer are migratable during said plasma processing.

[c18] 18. The method of claim 12, wherein at least one of said first grid and said second grid comprises a metal grid that is a predetermined surface area of at least one of said first circuit design module and said second circuit design module.

[c19] 19. An electronic apparatus comprising:

at least one electronic chip, comprising:

a first circuit design module having a first grid;

a second circuit design module having a second grid; and

means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip.

[c20] 20. The electronic apparatus of claim 19, wherein at least one of said at least one electronic chip comprises a chip including a silicon on insulator (SOI) structure.